Exhibit 17

JEDEC STANDARD

DDR5 Registering Clock Driver Definition (DDR5RCD01)

JESD82-511

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

2.1 Pinout

Table 1 specifies the pinout for the DDR5RCD01.

Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA3_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA3_B	QB CA7_B	NU	**A**
B	QB CA1_A	V_{SS}	QB CA9_A	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	QB CA9_B	V_{SS}	QB CA1_B	**B**
C	QB CA6_A	V_{SS}	QB CA8_A	V_{DD}	ZQ CAL	SCL	DERROR_IN_A_n	DERROR_IN_B_n	SDA	V_{DDIO}	V_{DD}	QB CA8_B	V_{SS}	QB CA6_B	**C**
D	QB CA5_A	V_{SS}	QB CA2_A	V_{DD}	V_{DD}	V_{DD}			V_{DD}	V_{DD}	V_{DD}	QB CA2_B	V_{SS}	QB CA5_B	**D**
E	QB CA0_A	V_{SS}	QB CA4_A	V_{DD}	QBCK_A_c	QBCK_A_t	V_{SS}	V_{SS}	QBCK_B_t	QBCK_B_c	V_{DD}	QB CA4_B	V_{SS}	QB CA0_B	**E**
F	QBCS0_A_n	V_{SS}	QBCS1_A_n	V_{DD}			V_{DD}	V_{DD}			V_{DD}	QBCS1_B_n	V_{SS}	QBCS0_B_n	**F**
G	QA CA11_A		QA CA13_A	V_{DD}	QDCK_A_c	QDCK_A_t	V_{SS}	V_{SS}	QDCK_B_t	QDCK_B_c	V_{DD}	QA CA13_B		QA CA11_B	**G**
H	QA CA9_A	V_{SS}	QA CA12_A	V_{DD}	**RFU**	**RFU**	V_{DD}	V_{DD}	**RFU**	**RFU**	V_{DD}	QA CA12_B	V_{SS}	QA CA9_B	**H**
J	QA CA10_A	V_{SS}	QA CA3_A	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	QA CA3_B	V_{SS}	QA CA10_B	**J**
K	QA CA6_A		QA CA7_A	V_{DD}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{DD}	QA CA7_B		QA CA6_B	**K**
L	QA CA1_A		QA CA4_A	V_{DD}	QA CA2_A	QA CA8_A	V_{SS}	V_{SS}	QA CA8_B	QA CA2_B	V_{DD}	QA CA4_B		QA CA1_B	**L**
M	QA CA5_A	V_{SS}	QA CA0_A	V_{DD}	QACK_A_c	QACK_A_t	V_{DD}	V_{DD}	QACK_B_t	QACK_B_c	V_{DD}	QA CA0_B	V_{SS}	QA CA5_B	**M**
N	QACS0_A_n	V_{SS}	QACS1_A_n	V_{DD}			V_{SS}	V_{SS}			V_{DD}	QACS1_B_n	V_{SS}	QACS0_B_n	**N**
P		V_{SS}			QCCK_A_c	QCCK_A_t	QLBD	QLBS	QCCK_B_t	QCCK_B_c			V_{SS}		**P**
R	**BCS_A_n**	**BCOM1_A**	**BCOM2_A**	**BRST_A_n**	**BCK_A_c**	**BCK_A_t**	V_{SS}	V_{SS}	**BCK_B_t**	**BCK_B_c**	**BRST_B_n**	**BCOM2_B**	**BCOM1_B**	**BCS_B_n**	**R**
T	**BCOM0_A**	V_{DD}	V_{DD}	DCS1_A_n	QRST_A_n		DCK_t	DCK_c		QRST_B_n	DCS0_B_n	V_{DD}	V_{DD}	**BCOM0_B**	**T**
U	DCA0_A	V_{SS}	DCS0_A_n	DLBD_A	DLBS_A	ALERT_n			DRST_n	DLBS_B	DLBD_B	DCS1_B_n	V_{SS}	DPAR_B	**U**
V	DCA1_A	V_{SS}	DCA3_A	V_{SS}	DPAR_A	V_{SS}	DCA6_A	V_{SS}	DCA1_B	V_{SS}	DCA3_B	V_{SS}	V_{SS}	DCA6_B	**V**
W	NU	DCA2_A	V_{SS}	DCA4_A	V_{SS}	DCA5_A	V_{SS}	DCA0_B	V_{SS}	DCA2_B	V_{SS}	DCA4_B	DCA5_B	NU	**W**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	

Table 2 — Terminal functions

Signal Group	Signal Name	Type	Description
Miscellaneous pins	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in RCD

1. SA pins are not required for DDR5RCD01 as the address will be hard-coded. Refer to Section 7.5.1, "Target Address," on page 78 for details.
2. SDA driver operation is dynamic. Depending on the SidebandBus mode of operation (I^2C RW25[5] = '0' or I3C Basic RW25[5] = '1'), and even on the specific step (byte or bit) of a SidebandBus transaction packet, the SDA output driver can operate either in open-drain mode or push-pull mode.
3. These inputs are 1.0-V inputs.

Naming Convention:

Input Example:
DCAy_N - where 'y' is the signal number and 'N' is the sub-channel.

Output Example:
QxCAy_N - where 'y' is the signal number, 'x' is the output copy (A or B) and 'N' is the sub-channel.

3 Device Standard

3.1 Description

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.

10 Electrical - Timing Requirements

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage[1]	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V
T_j	Junction temperature[2]		0	-	125	°C
T_{case}	Case temperature	Measurement procedure JESD51-2	-	-	103[3]	°C

1. DC bandwidth limited to 20 MHz.
2. For operation beyond Tj min and max datasheet values are not guaranteed and may de-rate. For operation above Tj max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C and 95 °C.
3. This spec is meant to guarantee a Tj of 125 °C by the DDR5RCD01. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a DDR5RCD01 shall not be higher than 125 °C.